JAF & IW

IN THE US PATENT & TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS & INTERFERENCES

APPLICANTS: KONISHI et al.

SERIAL #: 10/ 082,984 ATT. DOCKET: **542-007.3**

FILED: 25 FEB. 2002

TITLE: LIQUID CRYSTAL DISPLAY

EXAMINER: George Wang ART UNIT: 2871

BRIEF ON APPEAL

10 NOV. 2004

Commissioner for Patents
PO BOX 1450
ALEXANDRIA VA 22313-1450

Sir:

Further to the Notice of Appeal mailed 8 JUNE 2004 and received 10 JUNE 2004, Applicants hereby submit this BRIEF ON APPEAL. Extensions of time from 10 AUG 2004 to 10 NOV. 2004 were previously obtained.

(1) REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Display, Inc., the assignee by virtue of the assignment recorded 25 FEB. 2002 at Reel 12650, Frame 0358.

(2) RELATED APPEALS & INTERFERENCES

Counsel is not aware of any related appeals or interferences.

(3) STATUS OF CLAIMS

Claims 1-6 are pending. All of claims 1-6 were finally rejected on DEC. 8, 2003.

(4) STATUS OF AMENDMENTS

No amendment was filed subsequent to the Final Rejection.

A Request for Reconsideration was filed JUNE 4, 2004 but the Advisory Action mailed JUNE 23, 2004 indicated that the Request did not place the application in condition for allowance.

(5) SUMMARY OF THE INVENTION

The invention is directed to an improved structure for a Thin-Film-Transistor (TFT) array substrate for a Liquid Crystal Display (LCD). In a matrix arrangement, source lines (9) run in one direction and gate lines (2) run in a direction orthogonal thereto. A terminal electrode (16) connects an external signal source to the source lines (9) via contact holes (13). Each transistor (17) responds to signals from adjacent source and gate lines and serves as a switching element to switch a pixel electrode (15) on and off. In order to protect the transistors (17) from possible damage due to electrostatic discharges during the fabrication process, a short-circuit ring (23) is formed, temporarily connected to the transistors (17), as shown in FIG. 5. Later, in order to disconnect the ring (23), the array substrate is sliced or chamfered along a cutting line (24), as indicated by the diagonal in FIG. 8(b).

In prior art structures (FIGS. 4-8), the electrode layers were arranged such that, when the chamfering occurred, portions of source electrodes (9) tended to peel off or "exfoliate" and cause short-circuits between parallel gate lines (2). According to the modified structure (FIGS. 1-3) of the present invention, an insulating layer (4), such as silicon nitride, is interposed between a first metallic line (9) and a second metallic line (3), in order to minimize exfoliation of the second metallic line (3). Therefore, the structure of the present invention prevents short circuits, improves LCD reliability, reduces a need for highly accurate cutting and chamfering equipment during manufacturing, and reduces generation of waste material during manufacturing.

(6) ISSUES

Does a structure including a "terminal electrode" for one purpose suggest a structure including a "terminal electrode" for a different purpose?

Does positioning of an insulating layer for the purpose of improving storage capacitance suggest similar positioning of an insulating layer for a mechanical protection purpose?

Is a recitation of the functional effect of a structure merely an immaterial "product by process" limitation?

Can structural features of three references be selectively combined in an attempt to reach the claimed structure, if none of the three references recognizes the specific problem which is solved by the claimed structure?

(7) GROUPING OF CLAIMS

The claims form a single group, collectively rejected under section 103, based on a combination of US patents 5,546,204 (ELLIS), 5,724,107 (NISHIKAWA) and 5,771,083 (FUJIHARA). Dependent claims 2-6 set forth alternative embodiments of the basic structure recited in independent claim 1.

(8) ARGUMENT

None of the three references, relied upon to support the section 103 rejection, recognize that metallic fragments, created during manufacturing, threaten reliability of a completed TFT substrate for a liquid crystal display (LCD). Although there may be *incidental* similarities between the claimed invention and respective structural features of the three references, this does not provide sufficient motivation to combine those features in the manner suggested by the Examiner.

DOES A STRUCTURE INCLUDING A "TERMINAL ELECTRODE" FOR ONE PURPOSE SUGGEST A STRUCTURE INCLUDING A "TERMINAL ELECTRODE" FOR A DIFFERENT PURPOSE?

The final rejection, page 3, paragraph 2, concedes that the primary reference, FUJIHARA USP 5,771,083, "fails to specifically disclose" that a "terminal forming area is provided with a terminal electrode for connecting the gate or source line to at least one external signal source" as recited in main claim 1, but the final rejection attempts to fill this gap by citing the terminal electrode 14C shown in FIG. 6 of the NISHIKAWA USP 5,724,107 and described at NISHIKAWA col. 7, line 52 through col. 8, line 22. However, the NISHIKAWA terminal electrode does not connect to source or gate lines, but rather to storage capacitors 40, and thus is apparently intended for a different purpose than the terminal electrode 16 of the present invention, which applies the external signal to the source line (9) to, in turn, cause the Thin-Film-Transistor (17) to switch the pixel electrode (15). NISHIKAWA does not have the same kind of "terminal electrode" as the present invention, so that there is no motivation (as contended on page 4 of the final rejection) to try to combine NISHIKAWA's "terminal electrode" into the FUJIHARA structure, nor would such a combined structure function the same as the structure recited in claim 1, i.e. with the external signal being applied to the source line or gate line to actuate the switching element controlling the pixel electrode.

DOES POSITIONING OF AN INSULATING LAYER FOR THE PURPOSE OF IMPROVING STORAGE CAPACITANCE SUGGEST SIMILAR POSITIONING OF AN INSULATING LAYER FOR A MECHANICAL PROTECTION PURPOSE?

Claim 1 recites that "an insulating layer is interposed between the first metallic line and the second metallic line and serves, during fabrication of said display, to minimize exfoliation of said second metallic line" and page 4 of the

final rejection alleges that NISHIKAWA would motivate one to position an insulating layer in this manner (e.g. in the FUJIHARA structure) "to provide control over the storage capacitor." Specification page 12, lines 11-14, state that "by the gate insulating layer 4 covering the supplementary line 3, peeling of the supplementary line 3, as well as generation of peeled metal pieces can be decreased" which is clearly a **mechanical** protection purpose. It is respectfully submitted that the NISHIKAWA teaching concerning how to improve capacitor performance would not suggest adding such a feature to the FUJIHARA structure, where storage capacitors 40 are not of such importance, and the NISHIKAWA structure does not suggest the specific structure recited in the last paragraph of claim 1, much less the even more specific structures recited in claims 3-4 (first metallic line connected to the source line) or in claims 5-6 (second metallic line connected to the gate line).

IS A RECITATION OF THE FUNCTIONAL EFFECT OF A STRUCTURE MERELY AN IMMATERIAL "PRODUCT BY PROCESS" LIMITATION?

Claim 1 was amended on AUG. 29, 2003 to point out the inherent mechanical protection advantage of placing the insulating layer 4 **over** the second metallic line (rather than **under** the second metallic line, as shown in FIG. 8b) "to minimize exfoliation of the second metallic line, and short circuits resulting from such exfoliation" as discussed on specification page 12. Paragraph 5 of the final rejection dismissed this wording as a "product by process" limitation and asserted that the structure recited in claim 1 is "the same as or obvious from a product of the prior art." In fact, the structure is not "**the same as** a product of the prior art"; otherwise, there would be a section 102 rejection in this case. In fact, the structure is not "**obvious from** a product of the prior art" because the three cited references fail to teach a structure which, during manufacturing, minimizes production of metal shavings.

CAN STRUCTURAL FEATURES OF THREE REFERENCES BE SELECTIVELY COMBINED IN AN ATTEMPT TO REACH THE CLAIMED STRUCTURE, IF NONE OF THE THREE REFERENCES RECOGNIZES THE SPECIFIC PROBLEM WHICH IS SOLVED BY THE CLAIMED STRUCTURE?

The First Action in this application made a section 103 rejection of claims 1-6, based upon a combination of ELLIS/HONEYWELL (U.S.P. 5,546,204), showing liquid crystal interposed between a TFT substrate and a counter substrate, and FUJIHARA/SHARP (U.S.P. 5,771,083), alleged to show all the remaining features recited in claim 1. Neither ELLIS nor FUJIHARA mention the problem of metal shavings resulting from chamfering the edge of the substrate to remove the short-circuit ring 23, once the ring has served its purpose of protecting the thin-film transistors 17 during the manufacturing process. In response to the First Action, Applicants amended claim 1.

The Final Rejection, in spite of contending that the wording added to claim 1 was merely a "product by process" limitation not entitled to patentable weight, **also** contended that the new wording "necessitated" new grounds of rejection, namely adding reliance upon the newly-cited NISHIKAWA/SANYO U.S.P. 5,724,107, apparently cited for its terminal electrode connected to an external signal source. NISHIKAWA recognizes (col. 8, line 62, through col. 9, line 9) that there may be a problem of short circuits during manufacturing, arising from a storage capacitor electrode 40 coming into contact with a TAB (Tape Automated Bonding) but deals with that problem by not bringing the storage capacitor 40 to the edge of the substrate. Applicants have not found any mention of the problem of metal shavings, nor of how to structure the layers to minimize creation of metal shavings.

The Federal Circuit noted in Ruiz v. A.B. Chance Co., 234 F.3rd 654, 57 USPQ 2d 1161 (2000) that "In order to prevent a hindsight-based obviousness analysis, we have clearly established that the relevant inquiry for determining the scope and content

of the prior art is whether there is a reason, suggestion or motivation in the prior art or elsewhere that would have led one of ordinary skill in the art to combine the references." See also In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994).

In the final rejection, the FUJIHARA two-metallic-lines feature has been combined with the ELLIS liquid crystal feature and the NISHIKAWA storage capacitor connection to an external signal electrode feature, all without sufficient motivation for attempting the combination. Furthermore, none of these references recognize the problem of exfoliation leading to short circuits, and therefore none of them suggest that appropriate placement of the insulating layer will minimize such exfoliation.

CONCLUSION

The liquid crystal display structure recited in claims 1-6 provides significantly improved manufacturing yield and improved reliability in the product, and is an innovation worthy of protection. The need to discard completed LCD panels because short circuits cause an unacceptable fraction of "bad pixels" is a significant factor in the still-high cost of LCDs to consumers. None of FUJIHARA, ELLIS and NISHIKAWA, taken singly or in combination, suggest the structure recited. Therefore, the section 103 rejection is erroneous, and should be reversed.

Our check in the amount of $340 (FEE CODE 1402) is submitted herewith; if any additional fee is required, please charge to our Deposit Account 23-0442.

Respectfully submitted,

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(9) APPENDIX

1. A liquid crystal display comprising a TFT substrate, a counter substrate facing the TFT substrate, and liquid crystal interposed between the substrates, wherein

the TFT array substrate has a display area and a terminal forming area,

the display area is provided with a pixel electrode, a switching element connected to the pixel electrode, a gate line connected to the switching element and a source line connected to the switching element,

the terminal forming area is provided with a terminal electrode for connecting the gate line or source line to at least one external signal source, and

wherein

a first metallic line and a second metallic line, both connected to the terminal electrode via respective contact holes, are arranged below the terminal electrode at the terminal forming area, and an insulating layer is interposed between the first metallic line and the second metallic line and serves, during fabrication of said display, to minimize exfoliation of the second metallic line, and short circuits resulting from such exfoliation.

2. A liquid crystal display according to claim 1, wherein

the first metallic line is made from the same layer as that for the source line and

the second metallic line is made from the same layer as that for the gate line.

3. A liquid crystal display according to claim 1, wherein

the first metallic line is connected to the source line and

the second metallic line is arranged in a lower layer than the first metallic line.

4. A liquid crystal display according to claim 2, wherein

the first metallic line is connected to the source line and

the second metallic line is arranged in a lower layer than the first metallic line.

5. A liquid crystal display according to claim 1, in which the second metallic line is connected to the gate line and the second metallic line is arranged in a lower layer than the first metallic line.

6. A liquid crystal display according to claim 2, in which the second metallic line is connected to the gate line and the second metallic line is arranged in a lower layer than the first metallic line.

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Gentlemen:

Enclosed are our check # 26690 in the amount of $340 and the BRIEF ON APPEAL, in triplicate.

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I hereby certify that this document is being deposited, pursuant to 37 C.F.R. 1.8, in the U.S. Mail, first-class postage prepaid, addressed to the Commissioner for Patents, PO BOX 1450, Alexandria VA 22313-1450 on NOV. 10, 2004.

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